AMENDMENTS TO THE ABSTRACT

Please replace the Abstract with the following Abstract rewritten in an amended format:

~~A method and apparatus for a fast and automatic setting of the phase locked loop (PLL) output frequency that significantly improves linearity, locking range is well as spectrum purity, jitter and phase noise performances is disclosed. In one embodiment, a~~A phase lock loop (PLL) frequency synthesizer ~~is disclosed having~~includes a reconfigurable voltage controlled oscillator (VCO) with three modes of operation: a Linear-High-gain, Zero-gain, and Low-gain mode. During ~~a first tuning operation, the VCO work in a~~ the linear high gain mode, the VCO ~~enabling a totally~~enables an analogue self-calibration of the PLL over a wide frequency tuning range ~~and with a fast settling time~~. ~~During this operation the control~~ Control voltage at the input of the VCO is varied by the PLL to provide an ~~until the appropriate~~ output frequency ~~is found~~. ~~A method for providing a linear variation of the frequency over all the voltage tuning range during this mode is disclosed.~~ When the ~~N loop~~ PLL is locked, the VCO is ~~automatically~~ switched to the Zero-gain mode while maintaining the output ~~keeping its~~ frequency ~~unchanged. Its sensitivity to the noise in the control path is then practically eliminated and its phase noise performances significantly improved. If the frequency error and phase noise are sufficiently small for the considered application the tuning is stopped. If the error and phase noise are not sufficiently small the VCO is switched again to Low-gain mode and fine tuning adjustment of the output frequency is achieved.~~